IN THE CLAIMS

1. (Original) A method of forming a nearly planar dielectric film on a metal layer, comprising:

forming a metal layer having a predetermined maximum feature spacing;
forming an oxide layer on the metal layer using a TEOS-based procedure;
facet-etching the oxide layer; and
reflowing at least a portion of the oxide layer.

2. (Original) The method of claim 1, wherein forming the metal layer comprises forming metal layer with a maximum feature spacing of 0.3 microns.

3. (Original) The method of claim 1, wherein forming the metal layer comprises forming metal runners and wherein forming the oxide layer forms oxide on one or more sidewalls of the metal runners.

4. (Original) The method of claim 1, wherein forming the oxide layer comprises forming a portion of the oxide layer using a TEOS-based procedure at a first deposition rate and forming a portion of the oxide layer using a TEOS-based procedure at a second deposition rate which is less than the first deposition rate.

5. (Original) The method of claim 1, wherein forming the oxide layer comprises forming a portion of the oxide layer using a TEOS-based procedure at a first deposition rate having a tendency to form voids and forming a portion of the oxide layer using a TEOS-based procedure at a second deposition rate having a tendency to form substantially no voids or fewer voids than the first deposition rate.

6. (Previously Presented) The method of claim 1, further comprising facet etching the oxide layer to reduce severity of any trenches in the oxide layer overlying gaps between metal features in the metal layer.

7. (Previously Presented) A method comprising:

forming a metal layer having a predetermined maximum feature spacing of 0.3 microns;

forming a first oxide layer using a TEOS-based procedure at a first deposition rate on the metal layer;

forming a second oxide layer on the first oxide layer using a TEOS-based procedure at a second deposition rate which is less than the first deposition rate; and

facet etching the second oxide layer.

8. (Previously Presented) A method comprising:

forming a metal layer;

depositing a film resistant to lateral etching on the metal layer;

etching the metal layer to form a metal pattern having a predetermined maximum feature spacing of 0.3 microns;

forming a first oxide layer using a TEOS-based procedure at a first deposition rate on the metal pattern;

forming a second oxide layer on the first oxide layer using a TEOS-based procedure at a second deposition rate which is less than the first deposition rate; and

facet etching the second oxide layer.

9-14. (Canceled)

15. (Original) A method of making nearly planar dielectric films on a metal layer, where maximum feature spacing cannot be reduced because of lateral electrical coupling concerns, the method comprising:

forming a metal pattern with maximum feature spacing of about five microns;

forming an oxide spacer on one or more metal features of the metal layer to provide an effective space less than about five microns; and

executing a FLOW-FILL procedure to form a substantially void-free oxide layer on the metal layer and the oxide spacer.

16. (Original) The method of claim 15, wherein forming the metal pattern includes forming a metal layer; depositing a film resistant to lateral etching on the metal layer; and etching the metal layer to form the metal pattern.

17. (Original) The method of claim 16, wherein the film resistant to lateral etching is a TEOS, oxide-nitride film.

18. (Original) The method of claim 15, wherein forming the metal pattern includes forming a pattern including extensive serif features to avoid large open areas.

19. (Previously Presented) A method comprising:

depositing a dielectric material at a first deposition rate having a tendency to form voids; and

depositing a dielectric material on the deposited dielectric material at a second deposition rate having a tendency to form substantially no voids or fewer voids than the first deposition rate.

20. (Previously Presented) A method comprising:

depositing a dielectric material at a first deposition rate; and

depositing a dielectric material on the deposited dielectric material at a second deposition rate less than the first deposition rate.

21. (Previously Presented) A method comprising:

depositing a dielectric material using a deposition process having a first conformal tendency; and

depositing a dielectric material on the deposited dielectric material using a deposition process having a second conformal tendency greater than the first conformal tendency.

22. (Original) The method of claim 21:

wherein depositing a dielectric material using a deposition process having a first conformal tendency comprises depositing a dielectric material using a TEOS-based procedure at a first deposition rate; and wherein depositing a dielectric material using a deposition process having a second conformal tendency comprises depositing a dielectric material using a TEOS-based procedure at a second deposition rate lower than the first deposition rate.

23. (Original) A method of making an integrated circuit, comprising:

providing a first metal layout having a first pattern fill density;

generating a metal layout pattern based on the first metal layout and having a second pattern fill density greater than the first pattern fill density;

forming a metal pattern on a layer;

depositing a dielectric material on the metal pattern using a deposition process having a first conformal tendency; and

depositing a dielectric material on the deposited dielectric material using a deposition process having a second conformal tendency greater than the first conformal tendency.

24. (Original) A method of making an integrated circuit, comprising:

providing a first metal layout having a first pattern fill density;

generating a metal layout pattern based on the first metal layout and having a second pattern fill density greater than the first pattern fill density;

forming a metal pattern on a layer;

depositing a dielectric material on the metal pattern at a first deposition rate; and depositing a dielectric material on the deposited dielectric material at a second deposition rate less than the first deposition rate.

25. (Original) A method of making an integrated circuit, comprising:

providing a first metal layout having a first pattern fill density;

generating a metal layout pattern based on the first metal layout and having a second pattern fill density greater than the first pattern fill density;

forming a metal pattern on a layer;

forming a first oxide layer on the metal pattern using a TEOS-based procedure at a first deposition rate; and

forming a second oxide layer on the first oxide layer using a TEOS-based procedure at a second deposition rate lower than the first deposition rate.

26. (Previously Presented) A method comprising:

identifying and filling in open areas of a metal_layout with floating metal;

identifying and filling in notches of the metal layout; and

identifying and filling in corners of the metal layout.

27. (Previously Presented) A method comprising:

identifying and filling in one or more open areas of the metal layout with floating metal;

identifying and filling in one or more notches of the metal layout after identifying and filling in one or more open areas; and

identifying and filling in one or more corners of the metal layout after filling in one or more notches.

28. (Previously Presented) A method comprising:

identifying and filling in one or more notches of the metal layout;

identifying and filling in one or more corners of the metal layout; and

identifying and filling in between opposing edges of live metal regions of the metal layout.

29. (Previously Presented) A method comprising:

identifying and filling in one or more notches, inner lines, and corners of a metal_layout to define a first derivative metal layout pattern definition;

determining whether the first derivative metal layout pattern definition has a predetermined pattern fill density;

identifying and filling in one or more notches and corners of the metal layout to define a second derivative metal layout pattern definition;

determining whether the second derivative metal layout pattern definition has the predetermined pattern fill density; and

redefining one or more edges of the second derivative metal layout in response to determining that the second derivative metal layout does not have the predetermined pattern fill density.

30-32. (Canceled)

33-39. (Canceled)

40-42. (Canceled)

43. (Previously Presented) The method of claim 1, wherein forming the metal layer comprises:
identifying and filling in open areas of a metal layout with floating metal;
identifying and filling in notches of the metal layout; and
identifying and filling in corners of the metal layout.

44. (Previously Presented) The method of claim 7, wherein the TEOS-based procedure at the first deposition rate has a tendency to form voids and the TEOS-based procedure at the second deposition rate has a tendency to form substantially no voids or fewer voids than the first deposition rate.

45. (Previously Presented) The method of claim 7, further including:
reflowing at least a portion of the oxide layer; and
depositing a film resistant to lateral etching.

46. (Previously Presented) The method of claim 7, wherein forming the metal layer comprises
forming a first metal layer;
depositing a film resistant to lateral etching on the first metal layer; and
etching the first metal layer to form a metal pattern having a predetermined maximum feature spacing of 0.3 microns to form the metal layer.

47. (Previously Presented) The method of claim 7, wherein forming the metal layer comprises:

identifying and filling in open areas of a metal layout with floating metal;

identifying and filling in notches of the metal layout; and

identifying and filling in corners of the metal layout.

48. (Previously Presented) The method of claim 8, wherein the TEOS-based procedure at the first deposition rate has a tendency to form voids and the TEOS-based procedure at the second deposition rate has a tendency to form substantially no voids or fewer voids than the first deposition rate.

49. (Previously Presented) The method of claim 8, wherein forming the metal layer comprises:

providing a first metal layout having a first pattern fill density;

generating a metal layout pattern based on the first metal layout and having a second pattern fill density greater than the first pattern fill density;

forming a metal pattern on a layer;

depositing a dielectric material on the metal pattern at a first deposition rate; and

depositing a dielectric material on the deposited dielectric material at a second deposition rate less than the first deposition rate.

50. (Previously Presented) The method of claim 22, wherein the TEOS-based procedure at the first deposition rate has a tendency to form voids and the TEOS-based procedure at the second deposition rate has a tendency to form substantially no voids or fewer voids than the first deposition rate.

51. (Previously Presented) The method of claim 24:

wherein depositing the dielectric material on the metal pattern at the first deposition rate comprises using a TEOS-based procedure at the first deposition rate, with the first deposition rate having a tendency to form voids; and

wherein depositing the dielectric material on the deposited dielectric material at the second deposition rate comprises using a TEOS-based procedure at the second deposition rate, with the second deposition rate having a tendency to form substantially no voids or fewer voids than the first deposition rate.

52. (Previously Presented) The method of claim 25, wherein generating a metal layout pattern based on the first metal layout and having a second pattern fill density greater than the first pattern fill density, comprises:

identifying and filling in open areas of the metal layout with floating metal;
identifying and filling in notches of the metal layout; and
identifying and filling in corners of the metal layout.

The Examiner is invited to contact Applicant's Representatives at the below-listed telephone number if there are any questions regarding this Response or if prosecution of this application may be assisted thereby.

Respectfully submitted,

WERNER JUENGLING

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6951

Date May 9, 2005 By Sul Arora
Suneel Arora
Reg. No. 42,267

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 9 day of May, 2005.

Tina Kohout
Name

Signature